Low switching losses
Low reverse recovery charge
Distributed amplified gate for high di_T/dt

Fast Thyristor
Type TFI933-250-36

Mean on-state current		I_{TAV}	250 A
Repetitive peak off-state voltage		V_{DRM}	3000 ÷ 3600 V
Repetitive peak reverse voltage		V_{RRM}	
Turn-off time		t_q	63.0 μs
V_{DRM}, V_{RRM}, V	3200	3400	3600
Voltage code	32	34	36
T_j, °C	– 60 ÷ 125		

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	250 410	T_c= 92 °C; Double side cooled; T_c= 55 °C; Double side cooled; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	390	T_c= 92 °C; Double side cooled; 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	5.4 6.2	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
			5.7 6.5	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
I^2t	Safety factor	$A^2s{\cdot}10^3$	146 193	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
			133 176	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	3200÷3600	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	3300÷3700	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.75·V_{DRM} 0.75·V_{RRM}	T_j=$T_{j\,max}$; Gate open	

TRIGGERING				
I_{FGM}	Peak forward gate current	A	6	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	3	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	1000	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: $I_G=I_{FGM}$; $V_G=20$ V; $t_{GP}=50$ μs; $di_G/dt=2$ A/μs
THERMAL				
T_{stg}	Storage temperature	°C	– 60 ÷ 50	
T_j	Operating junction temperature	°C	– 60 ÷ 125	
MECHANICAL				
F	Mounting force	kN	9.0 ÷ 11.0	
a	Acceleration	m/s^2	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	3.20	$T_j=25$ °C; $I_{TM}=785$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.80	$T_j=T_{j\,max}$; $0.5\ \pi\ I_{TAV} < I_T < 1.5\ \pi\ I_{TAV}$	
r_T	On-state slope resistance, max	mΩ	2.400		
I_H	Holding current, max	mA	500	$T_j=25$ °C; $V_D=12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	70	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)]	V/μs	200, 320, 500, 1000	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	4.00 2.50 2.00	$T_j=T_{j\,min}$ $T_j=25$ °C $T_j=T_{j\,max}$	$V_D=12$ V; $I_D=3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 300 200	$T_j=T_{j\,min}$ $T_j=25$ °C $T_j=T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	10.00		
SWITCHING					
t_{gd}	Delay time, max	μs	1.38	$T_j=25$ °C; $V_D=1600$ B; $I_{TM}=I_{TAV}$; Gate pulse: $I_G=I_{FGM}$; $V_G=20$ V; $t_{GP}=50$ μs; $di_G/dt=2$ A/μs	
t_{gt}	Turn-on time	μs	4.00, 6.30, 8.00, 10.0		
t_q	Turn-off time[2)], max	μs	63.0	$dv_D/dt=50$ V/μs;	$T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; $di_R/dt=-10$ A/μs; $V_R=100$V; $V_D=0.67 \cdot V_{DRM}$
			80.0	$dv_D/dt=200$ V/μs;	
Q_{rr}	Total recovered charge, max	μC	500	$T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; $di_R/dt=-50$ A/μs; $V_R=100$ V	
t_{rr}	Reverse recovery time, typ	μs	5.0		
I_{rrM}	Peak reverse recovery current, max	A	200		

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0400	Direct current	Double side cooled
R_{thjc-A}			0.0880		Anode side cooled
R_{thjc-K}			0.0720		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0060	Direct current	
MECHANICAL					
w	Weight, typ	g	180		
D_s	Surface creepage distance	mm (inch)	19.44 (0.765)		
D_a	Air strike distance	mm (inch)	12.10 (0.476)		

PART NUMBERING GUIDE

TFI	933	250	36	A2	C3	N
1	2	3	4	5	6	7

1. TFI — Fast Thyristor
   TFIS — Fast Thyristor with Distributed Amplified Gate
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of off-state voltage
6. Group of turn-off time (dv_D/dt=50 V/μs)
7. Ambient conditions: N – normal; T – tropical

NOTES

[1] Critical rate of rise of off-state voltage

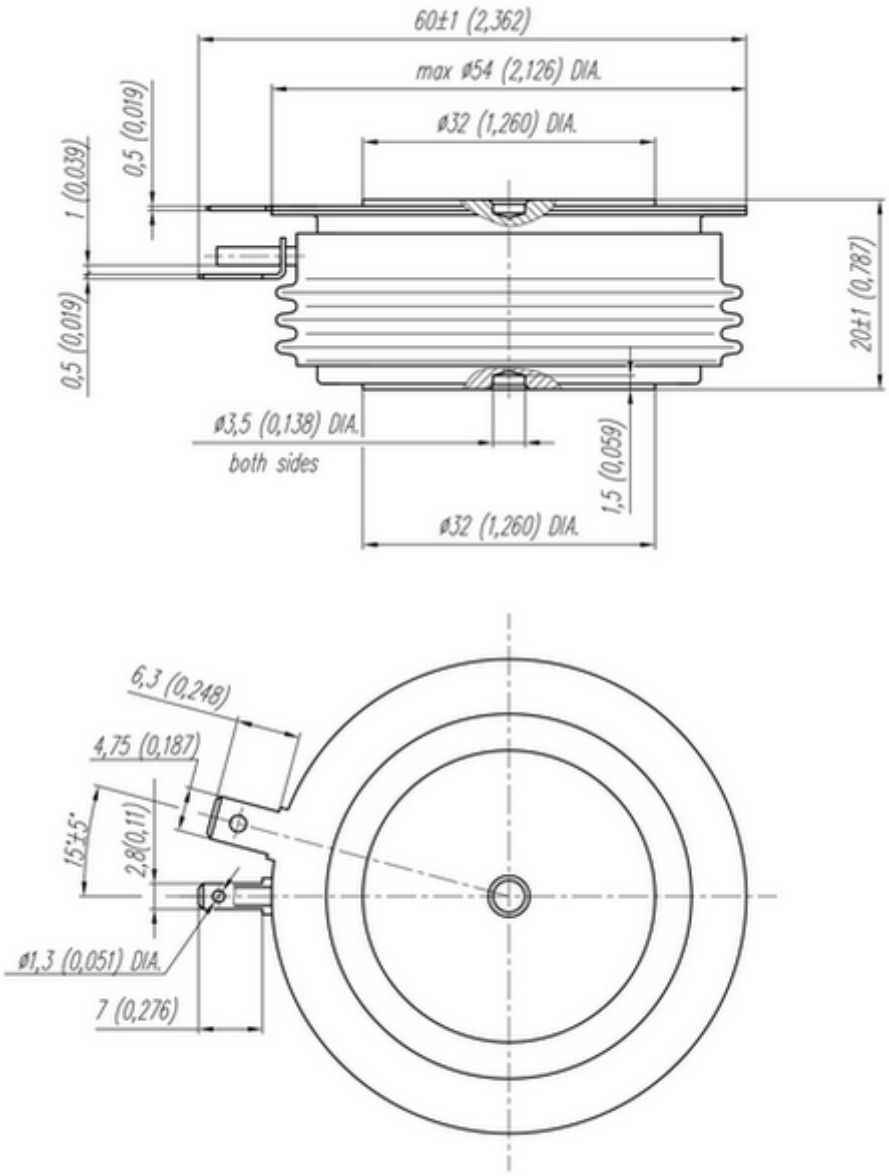
Symbol of group	P2	K2	E2	A2
$(dv_D/dt)_{crit}$, V/μs	200	320	500	1000

[2] Turn-off time (dv_D/dt=50 V/μs)

Symbol of group	C3
t_q, μs	63.0

OVERALL DIMENSIONS

Package type: T.B3



All dimensions in millimeters (inches)

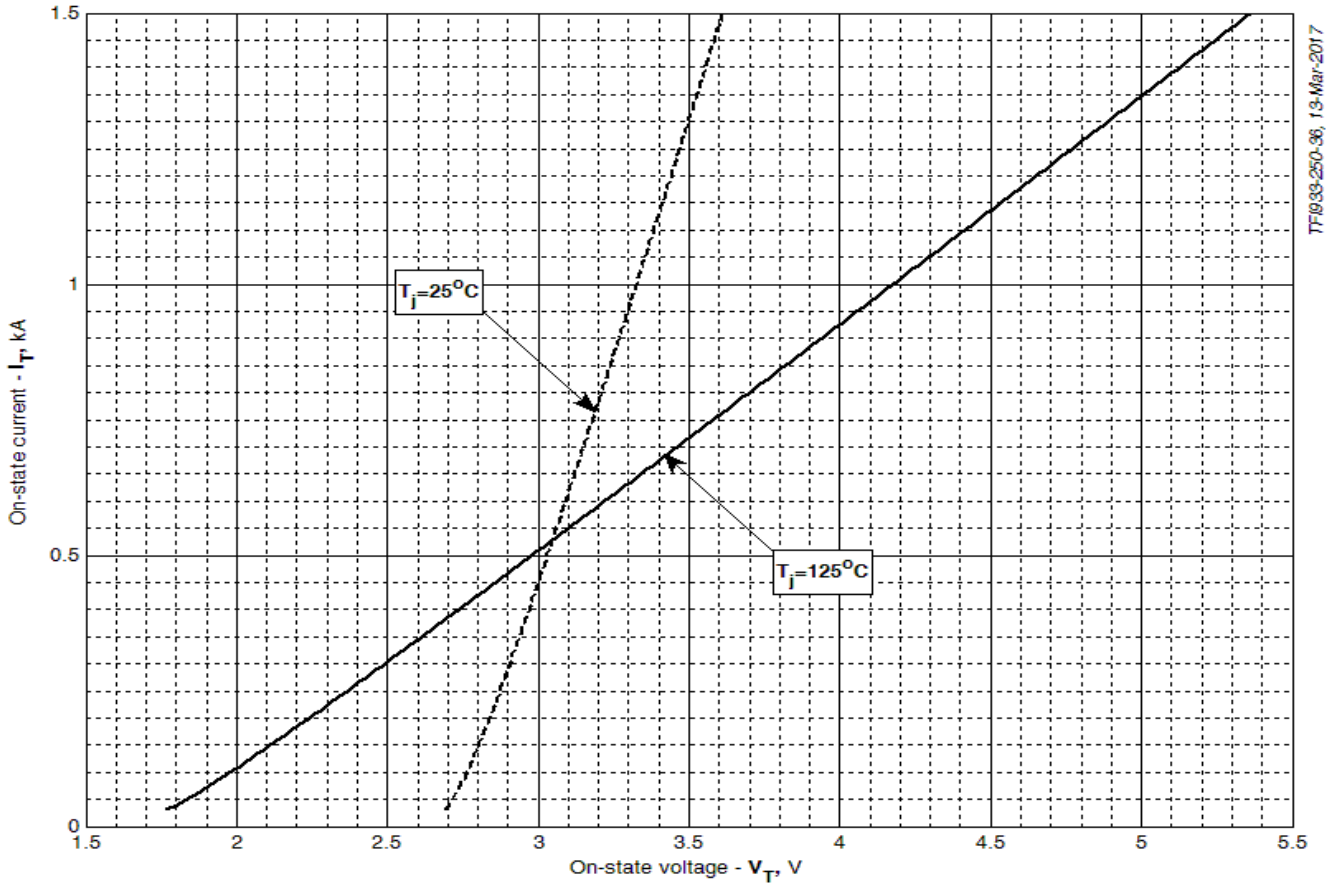


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	T_j = $T_{j\,max}$
A	2.624973	1.633421
B	0.532501	2.319300
C	-0.250342	-0.334349
D	0.340838	0.455213

On-state characteristic model (see Fig. 1)

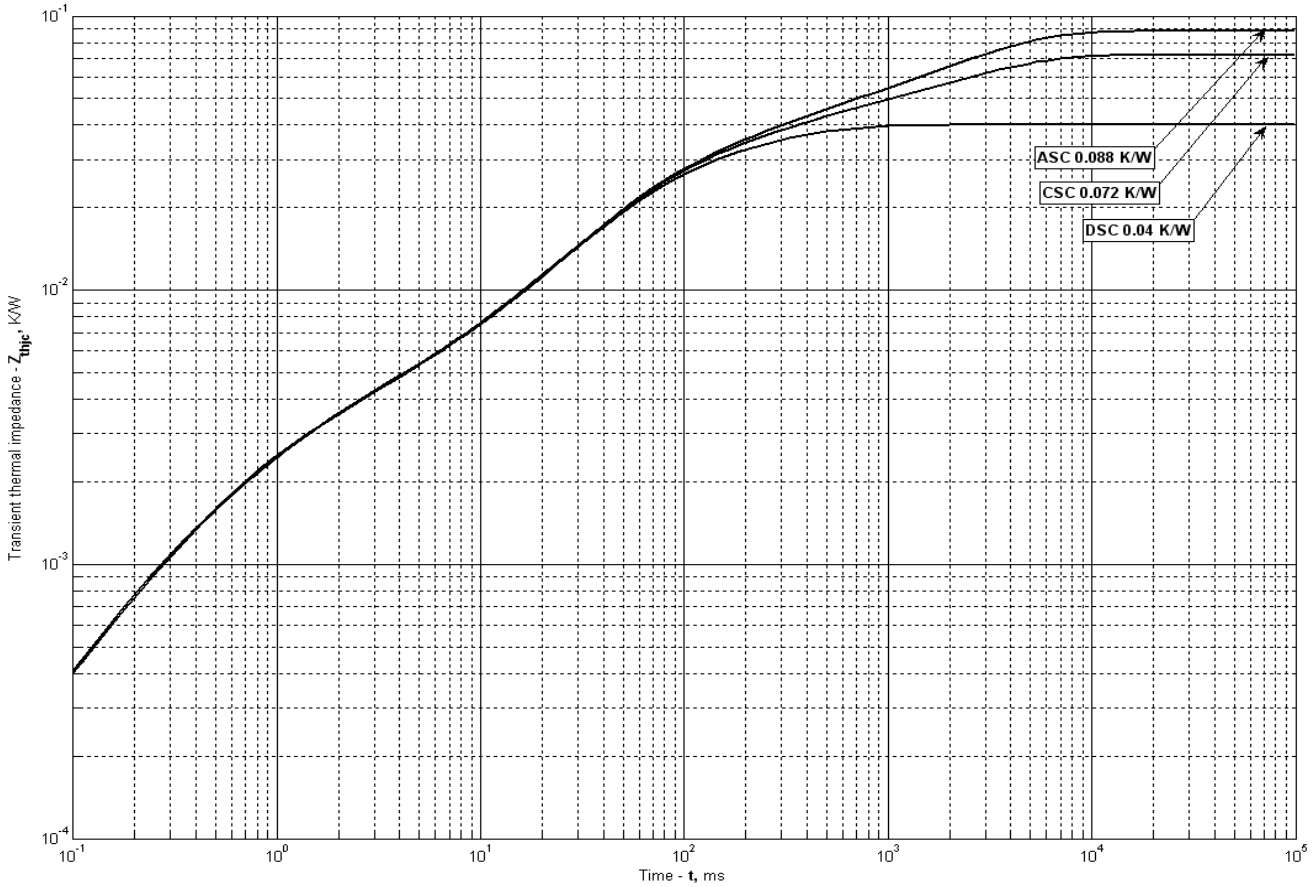


Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

$\mathbf{Z_{thjc}}$ = Thermal resistance at time t.

$\mathbf{R_i}$ = Amplitude of p_{th} term.

τ_i = Time constatnt of r_{th} term.

DC Double side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.01423	0.01906	0.003576	0.002535	-4.666e-005	0.0006479
τ_i, **s**	0.265	0.05901	0.03499	0.001252	0.000001	0.0002488

DC Anode side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.04804	0.001789	0.01342	0.02147	0.001374	0.001945
τ_i, **s**	2.651	0.4195	0.2622	0.05451	0.002585	0.0005847

DC Cathode side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.03216	0.01306	0.002934	0.02064	0.001493	0.001786
τ_i, **s**	2.647	0.2831	0.1455	0.05284	0.002255	0.0005519

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

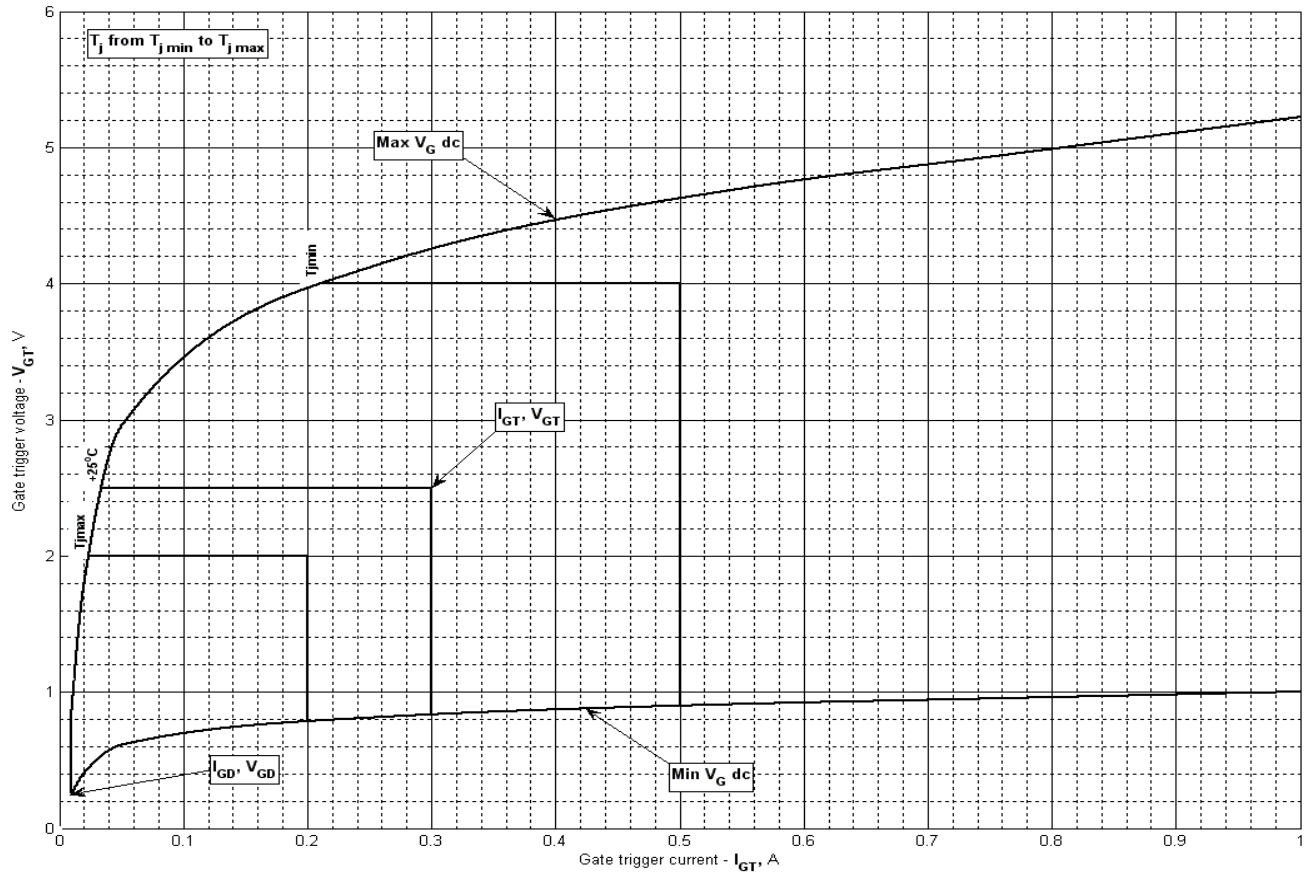


Fig 3 – Gate characteristics – Trigger limits

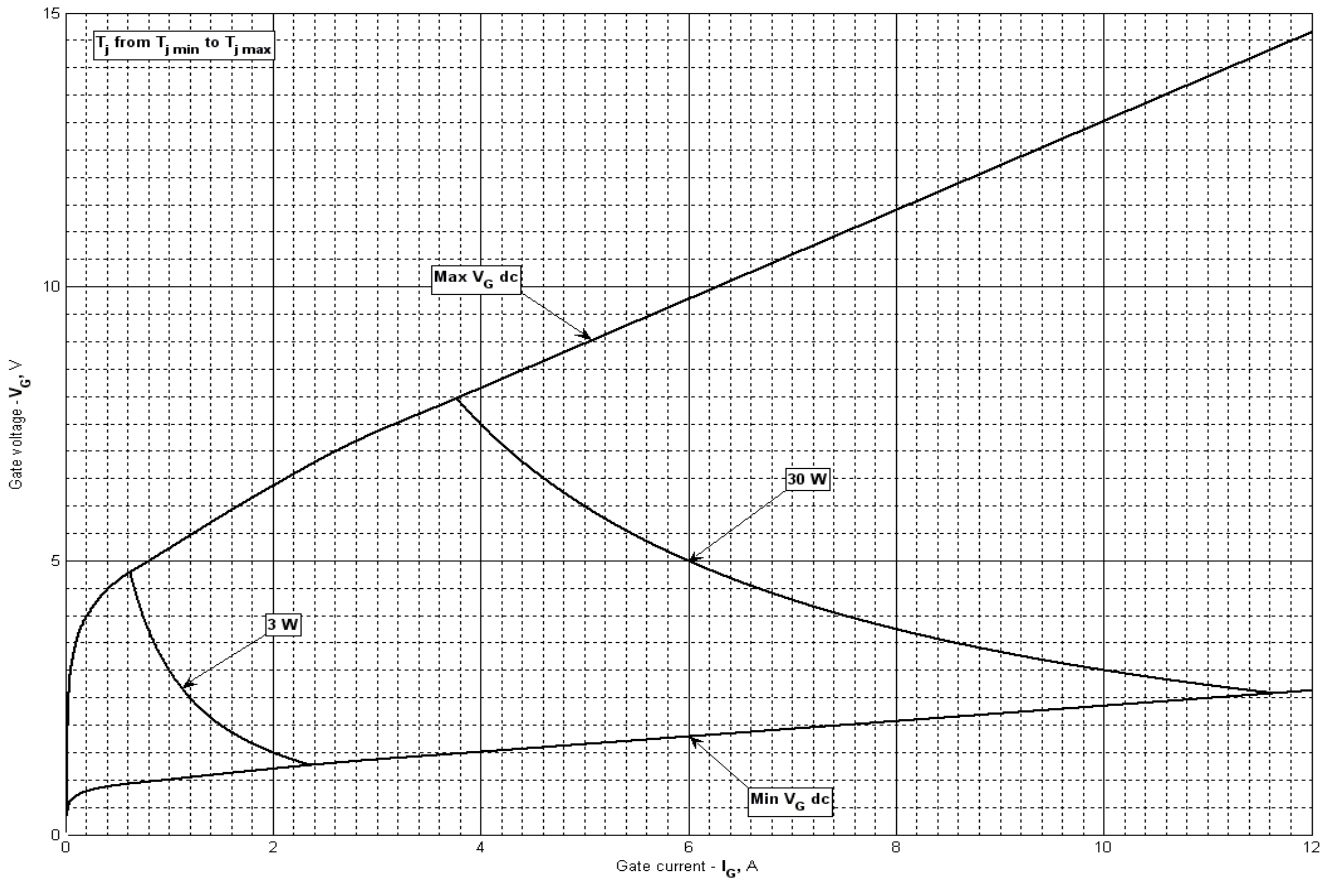


Fig 4 - Gate characteristics –Power curves

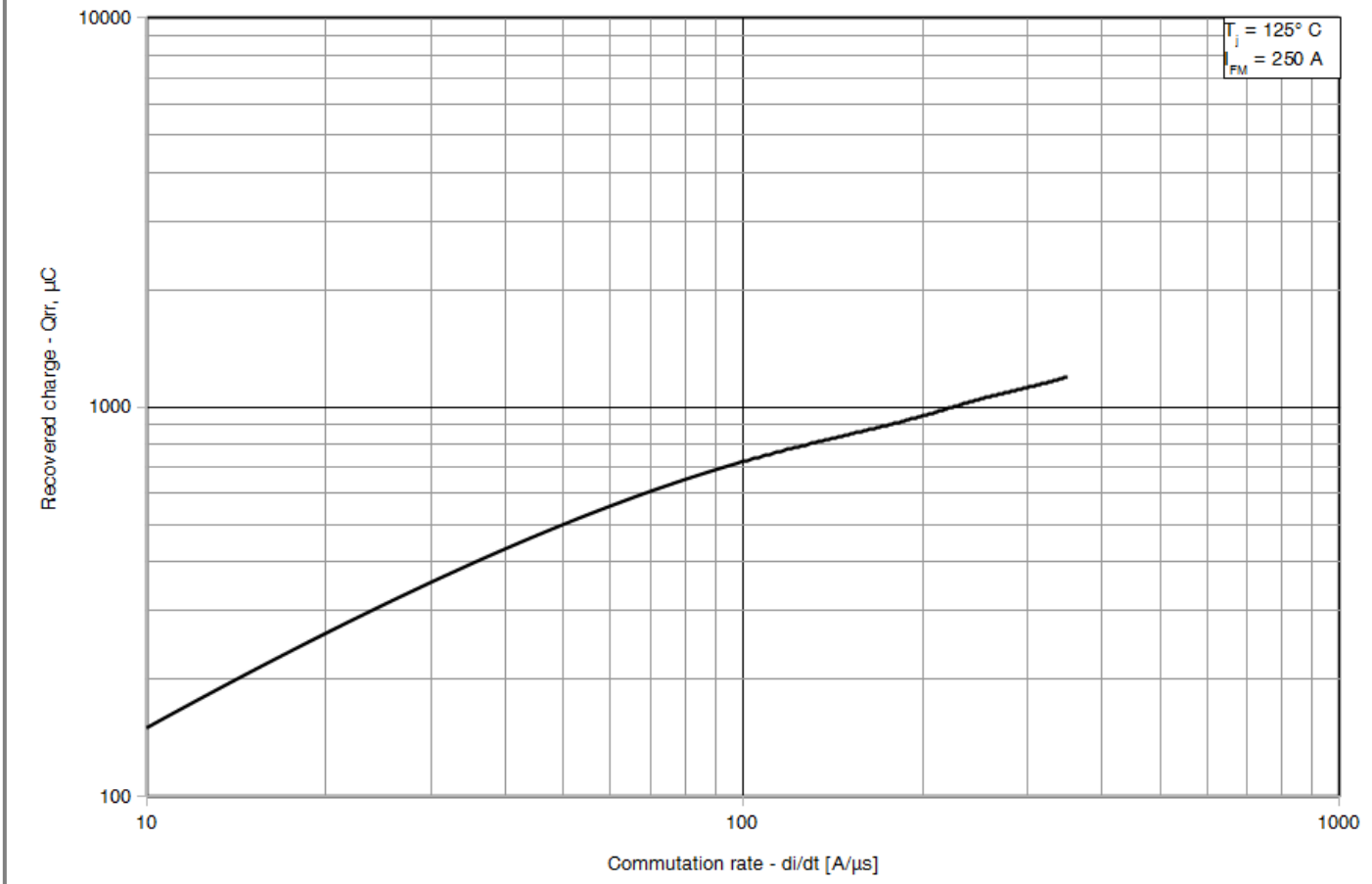


Fig 5 - Recovered charge, Q_{rr} (25% chord)

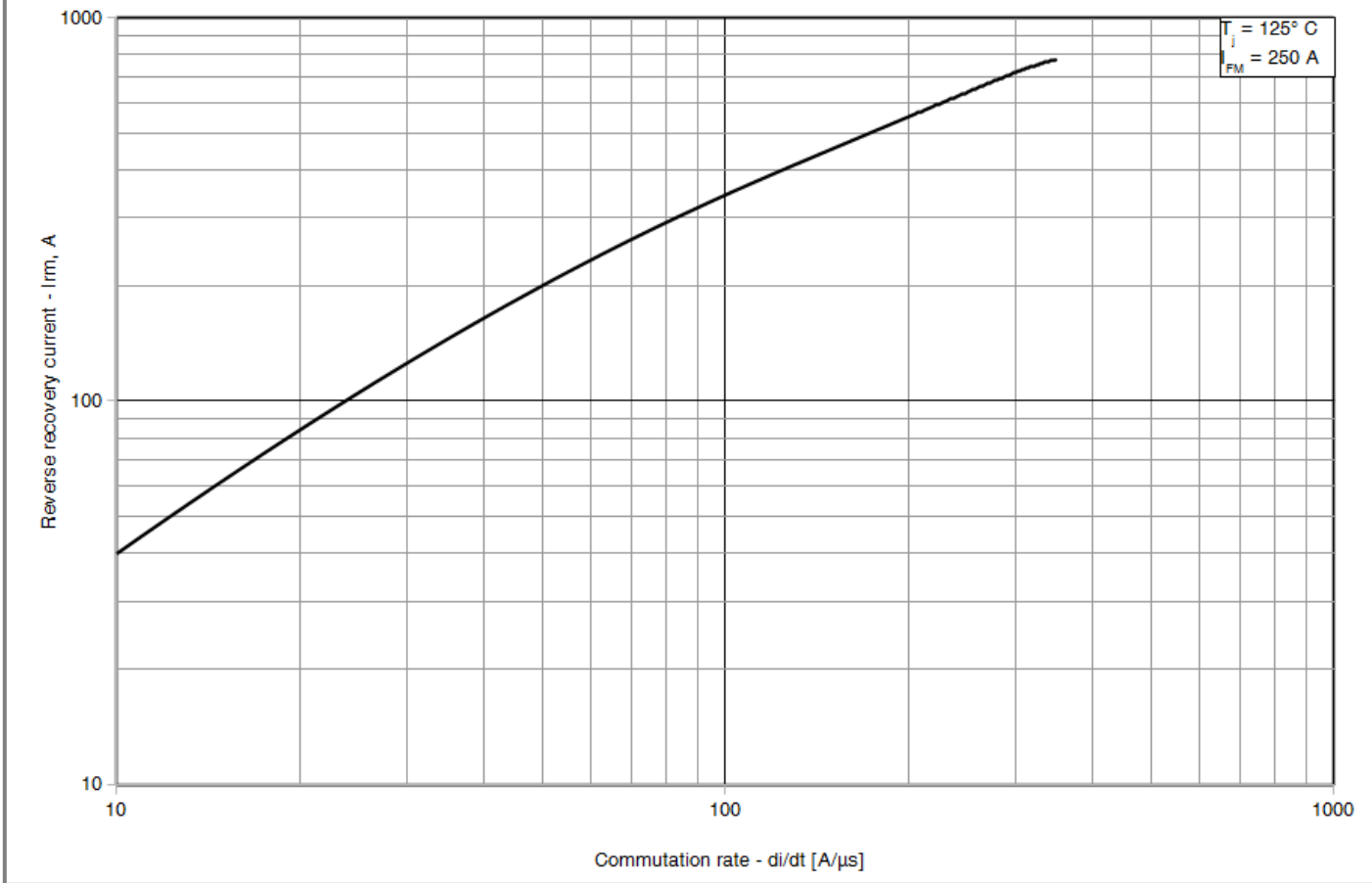


Fig 6 – Peak reverse recovery current, I_{rm}

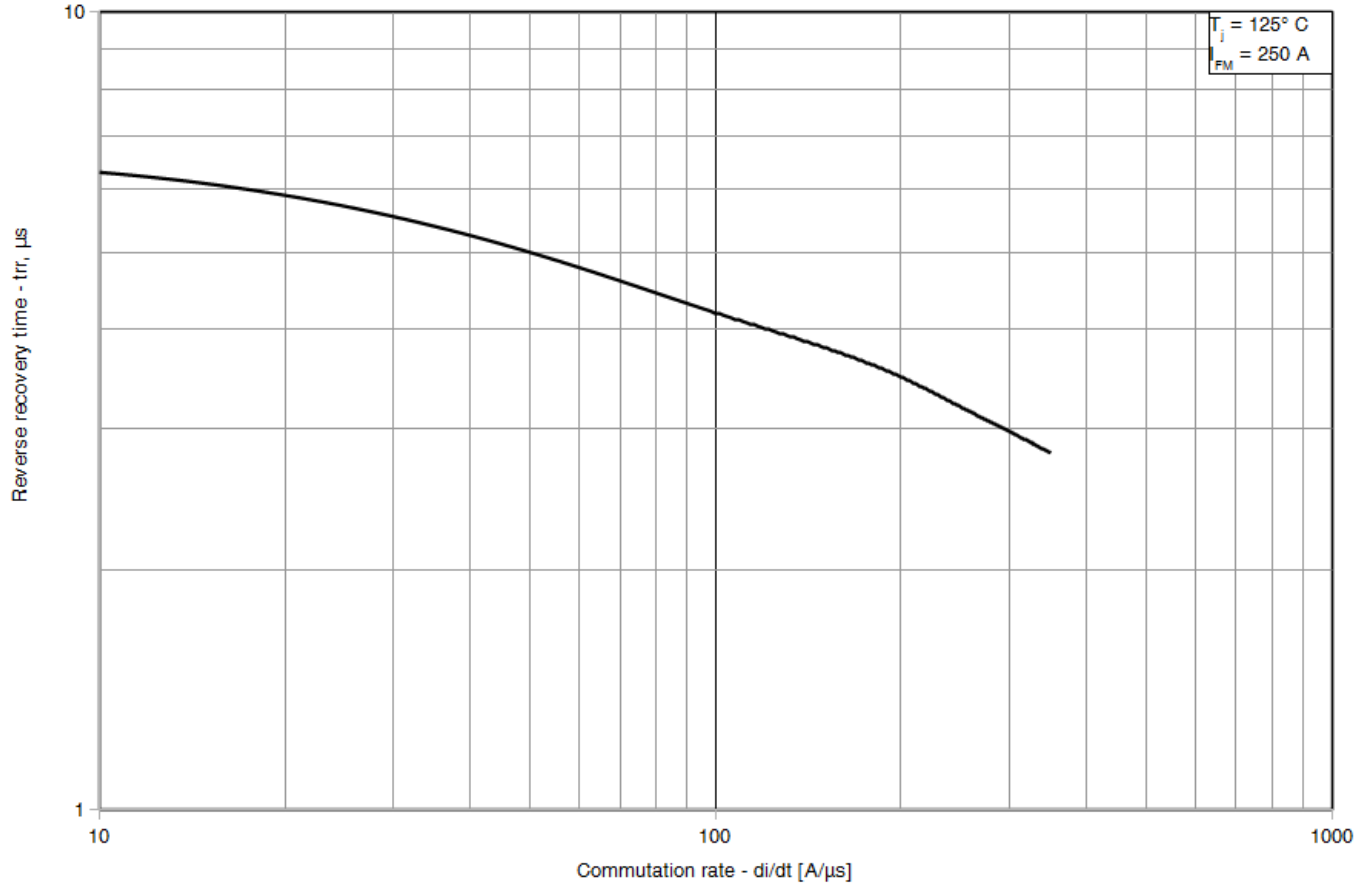


Fig 7 – Maximum recovery time, t_{rr} (25% chord)

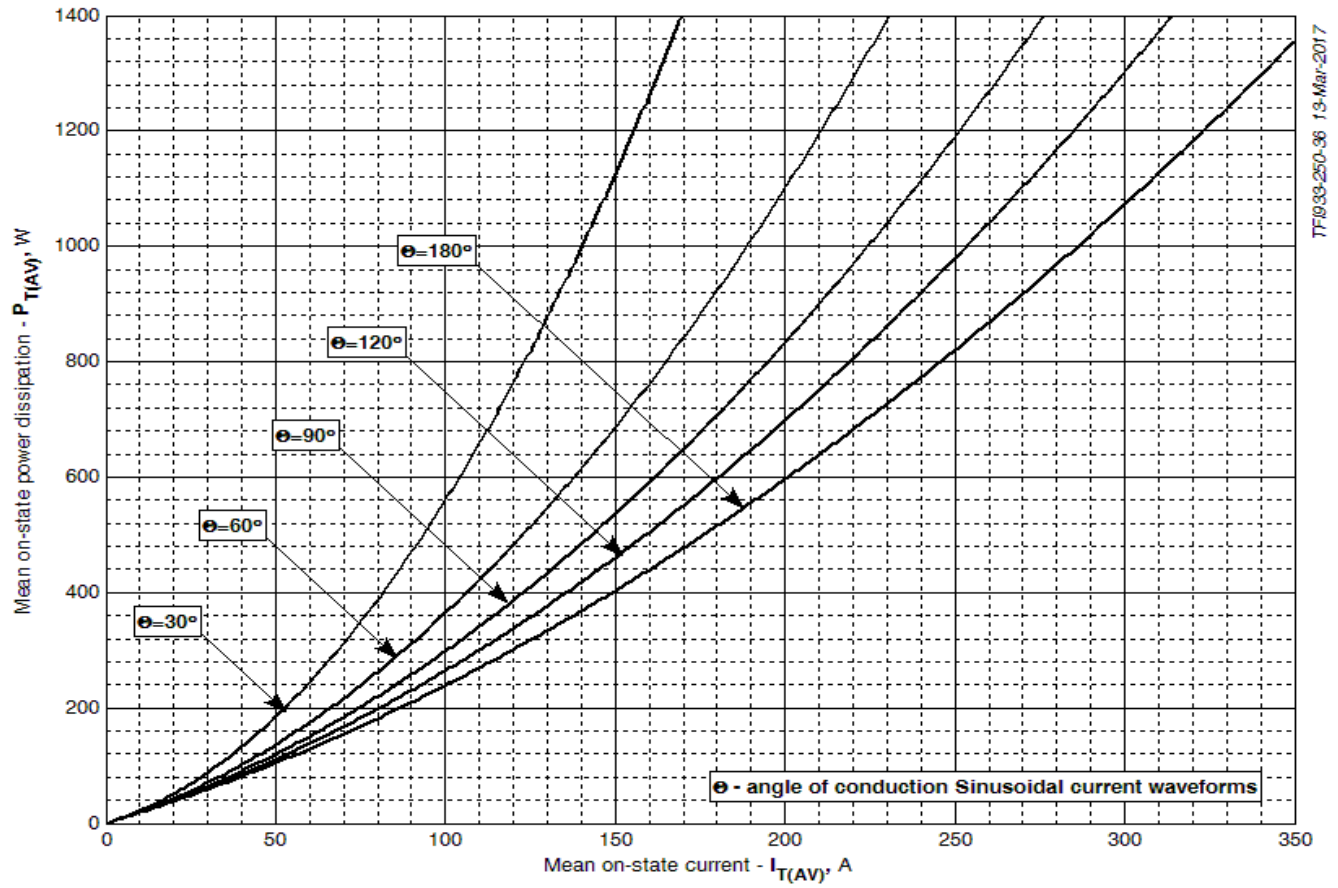


Fig 8 – On-state power loss (sinusoidal current waveforms)

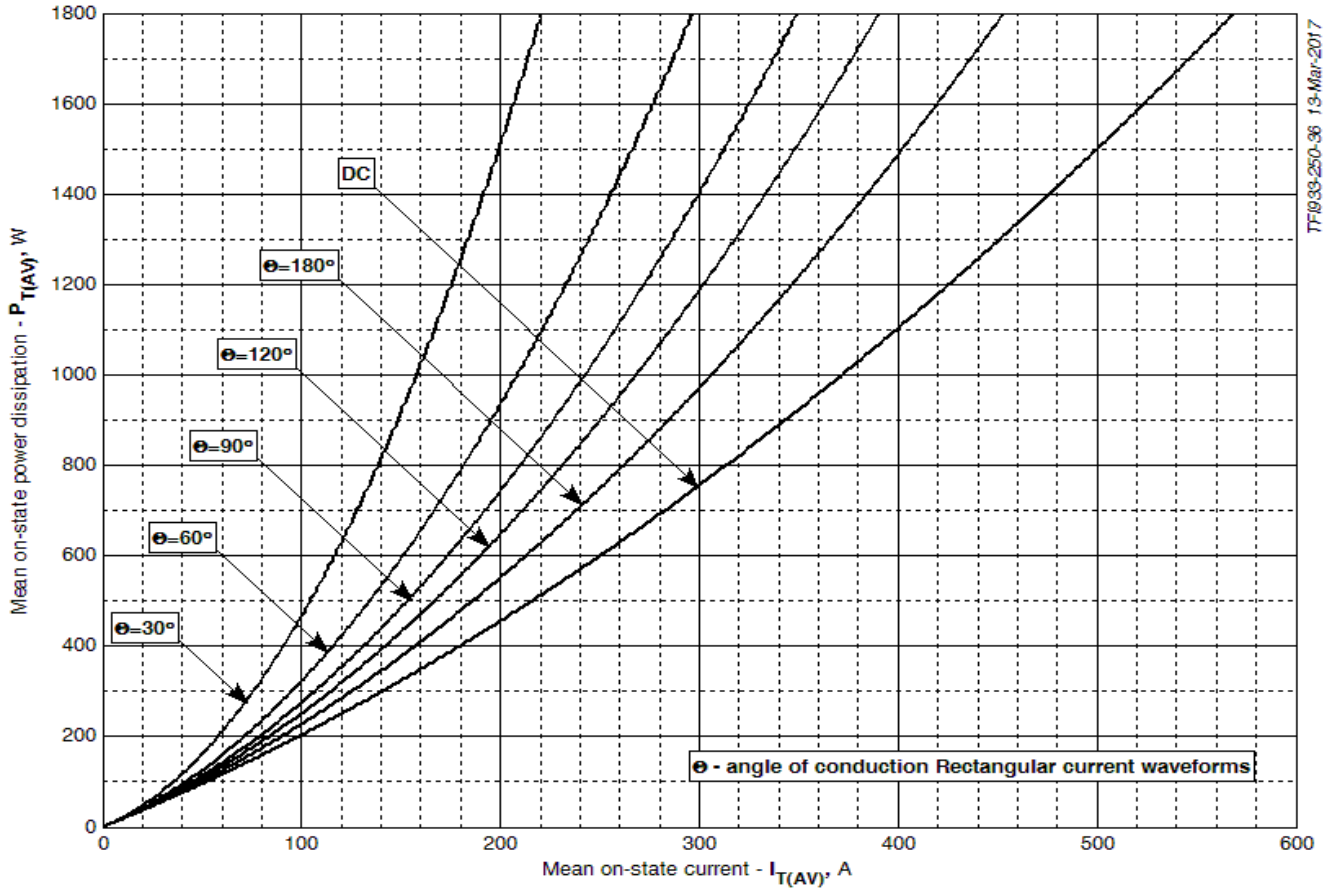


Fig 9 – On-state power loss (rectangular current waveforms)

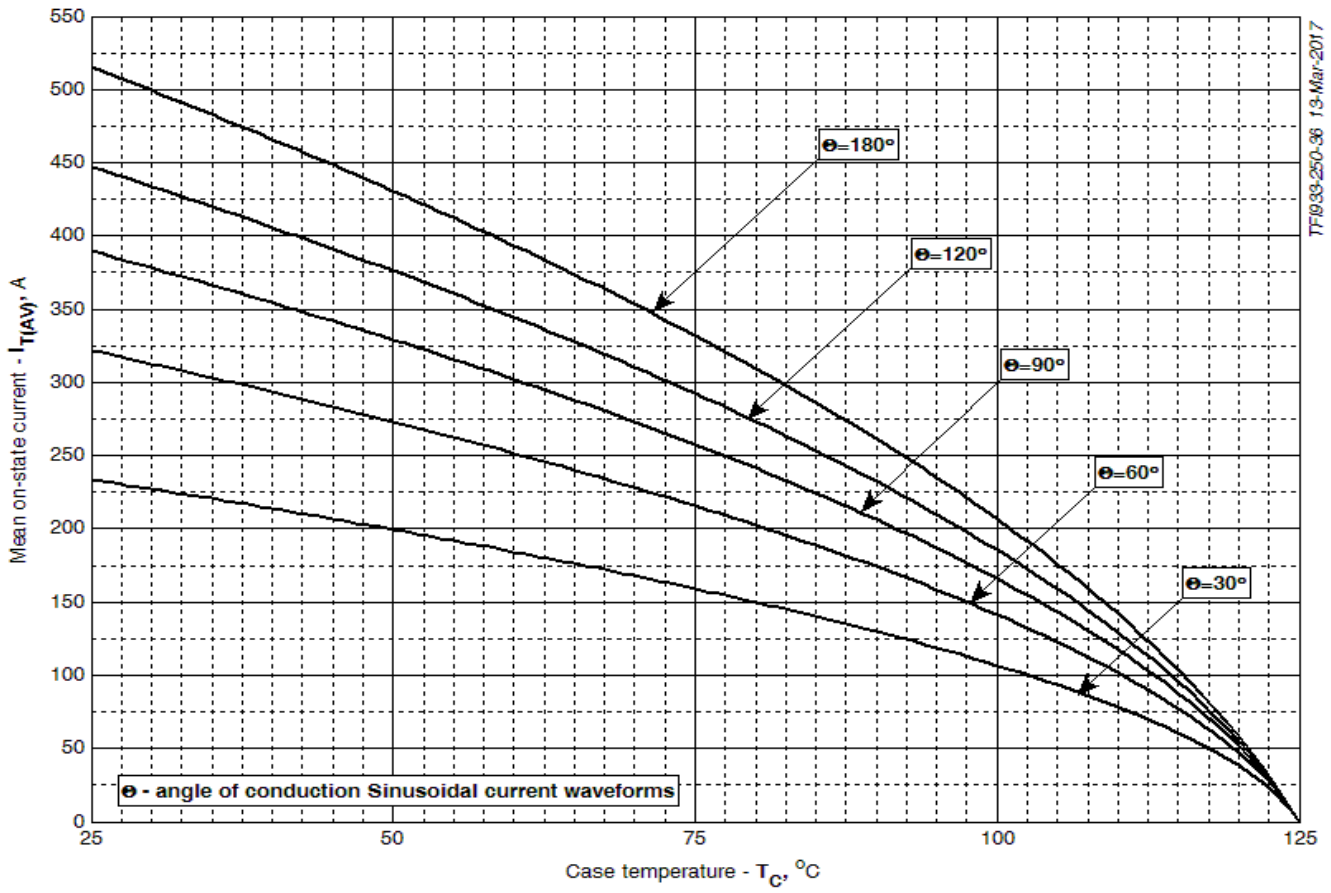


Fig 10 – Maximum case temperature DSC (sinusoidal current waveforms)

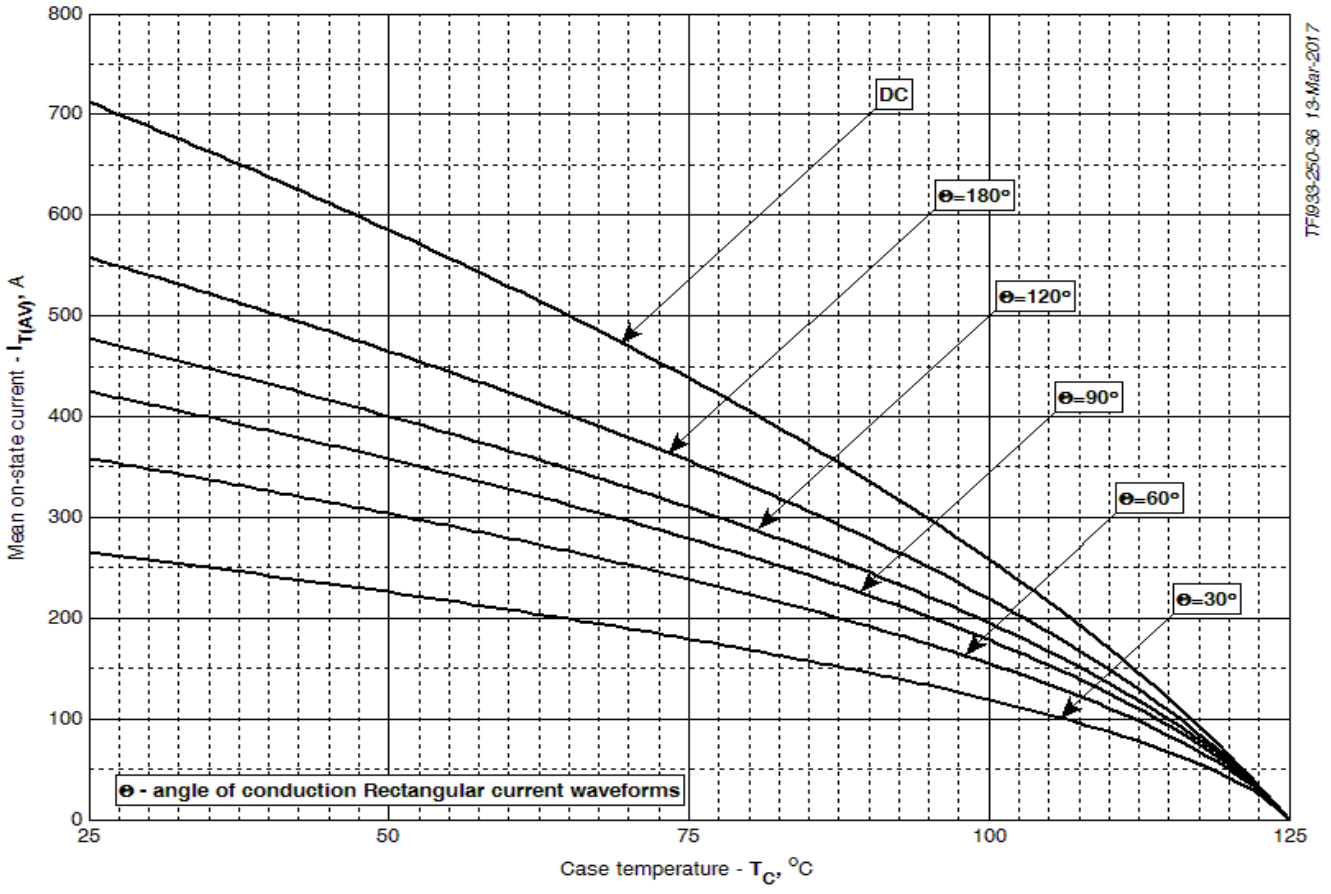


Fig 11 – Maximum case temperature DSC (rectangular current waveforms)

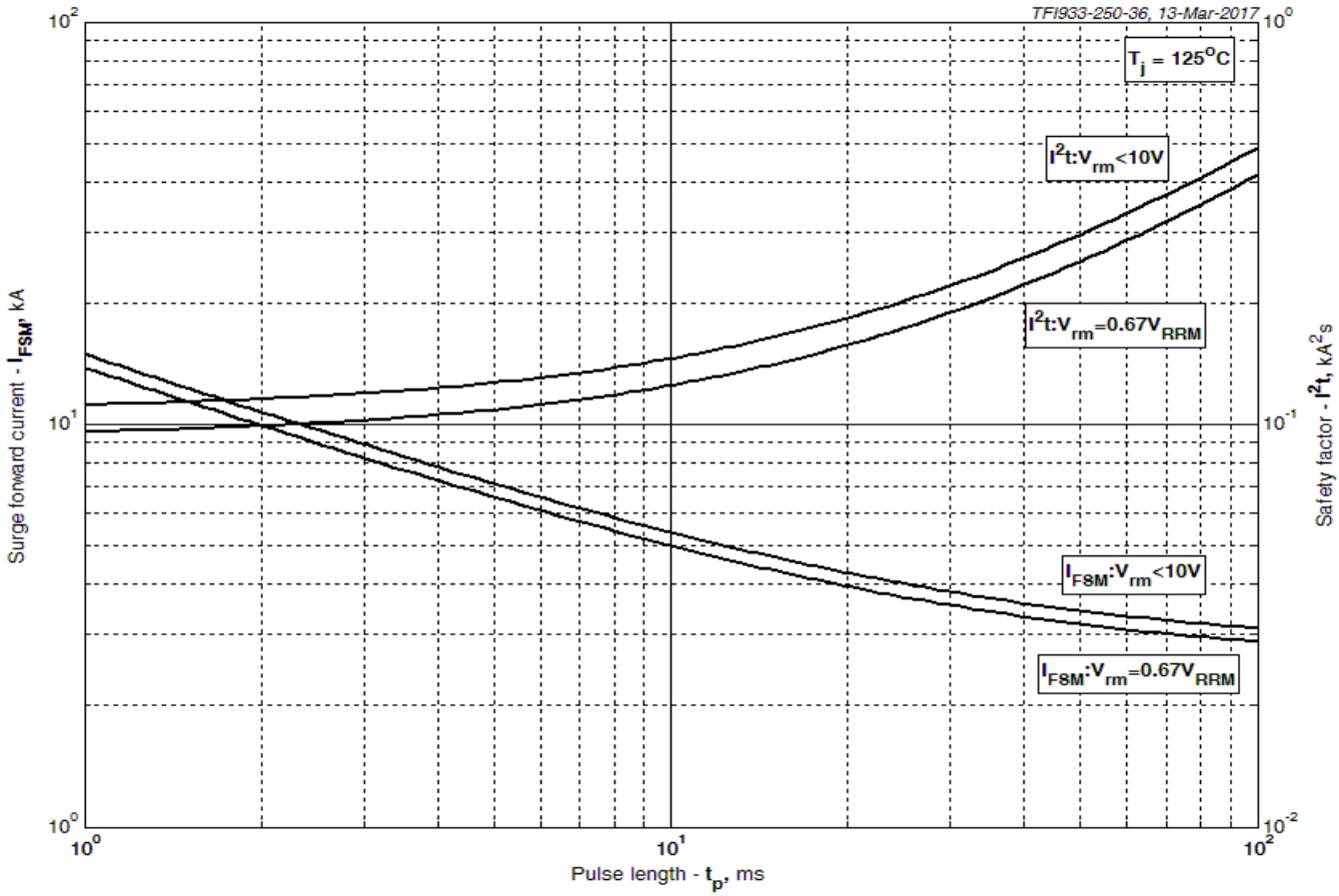


Fig 12 – Maximum surge and I^2t ratings

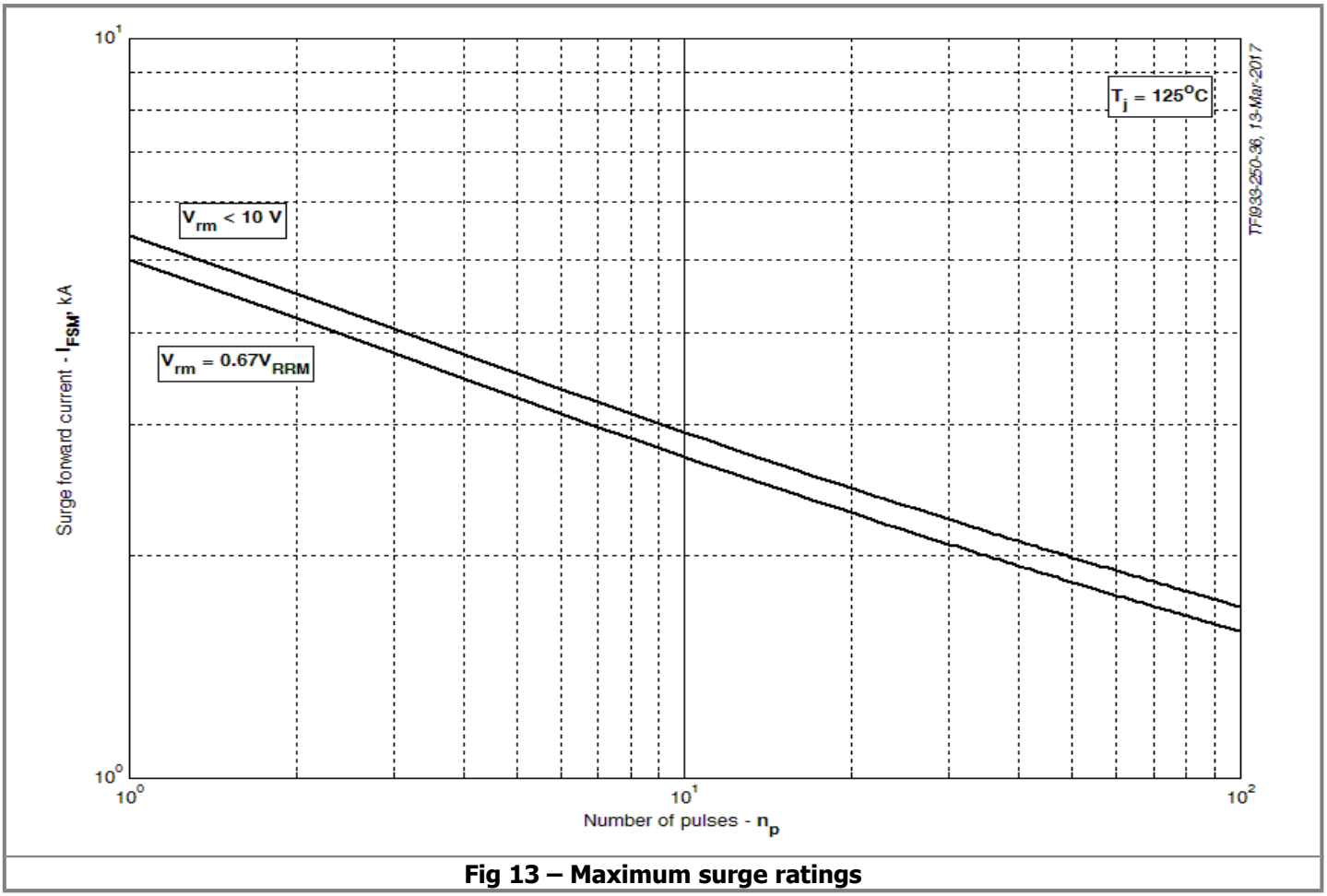


Fig 13 – Maximum surge ratings